查询HCT240供应商

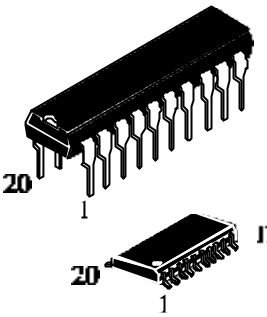
Octal 3-State Inverting Buffer/Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

The SL74HCT240 is identical in pinout to the LS/ALS240. The SL74HCT240 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

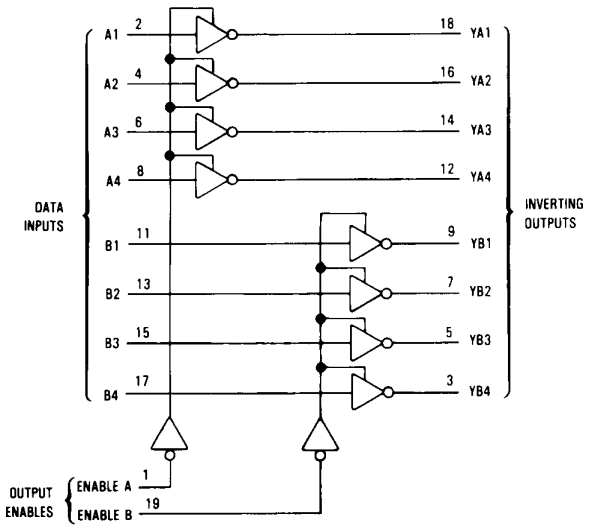
This octal inverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 µA



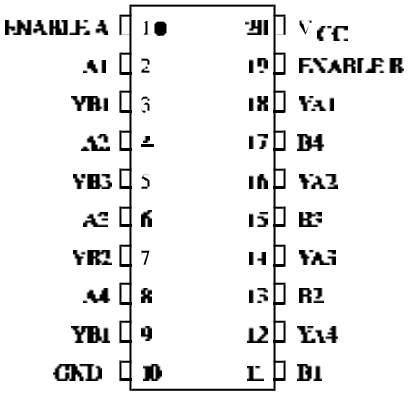
ORDERING INFORMATION
SL74HCT240N Plastic
SL74HCT240D SOIC
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A,B	YA,YB
L	L	H
L	H	L
H	X	Z

X = don' t care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V $\|I_{OUT}\| \le 20\ \mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}= V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}= V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{IN}=V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=V_{IH} $\|I_{OUT}\| \le 20\ \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{IN}= V_{IH} $\|I_{OUT}\| \le 6.0$ mA	4.5	0.26	0.33	0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum three State Leakage Current	Output in High-Impedance State V_{IN} = V_{IL} or V_{IH} V_{OUT}=V_{CC} or GND	5.5	±0.5	±5.0	±10.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0µA	5.5	4.0	40	160	µA
ΔI_{CC}	Additional Quiescent Supply Current	V_{IN} = 2.4 V, Any One Input V_{IN}=V_{CC} or GND, Other Inputs		≥-55°C		25°C to 125°C	mA
		I_{OUT}=0µA	5.5	2.9		2.4	

NOTE: Total Supply Current = $I_{CC} + \sum \Delta I_{CC}$

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5.0 V ± 10%, C_L=50pF, Input t_r=t_f=6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	20	25	30	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	25	31	38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{IN}	Maximum Input Capacitance	10	10	10	pF
C_{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Enable Output)	Typical @25°C, V_{CC}=5.0 V	pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	55	

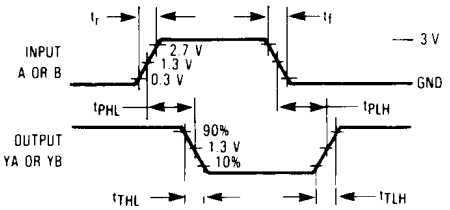


Figure 1. Switching Waveforms

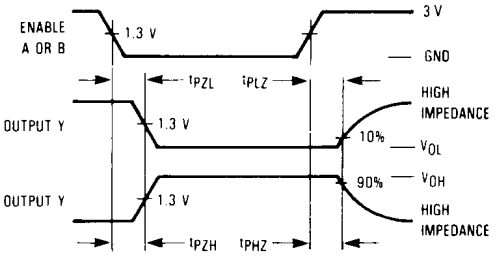


Figure 2. Switching Waveforms

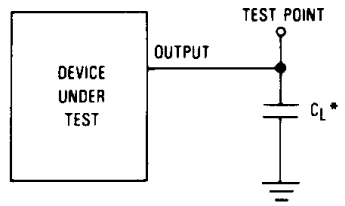


Figure 3. Test Circuit

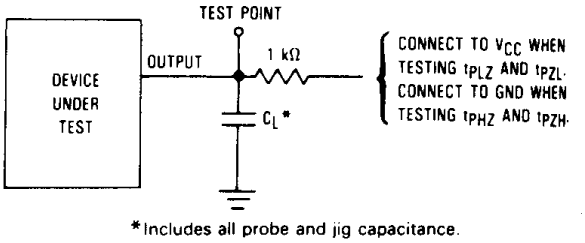


Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM

(1/8 of the Device)